TM-999
2562.000

Fermilab

DRIFT CHAMBER AMPLIFIER - DISCRIMINATOR CIRCUITS

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Introduction

This report describes an amplifier-discriminator system for four 60 cell bi-dimensional drift chambers located in the Muon Lab. The chamber employs flexible printed delay lines and conventional anode signal wires. The salient features of the chambers have been described previously.[1]

The delay-line amplifier is a discrete transimpedance type followed by polarity sensitive ECL discriminators and fixed pulse width output drivers. The anode-wire amplifier-discriminators are similar except for an ECL front end. The MC 10216 line receiver was the only integrated circuit employed. In this system it functions as an amplifer, positive or negative discriminator, voltage programmable monostable multivibrator, fixed pulse width generator and line driver.

The amplifier discriminators are mounted on 12.5 x 7 inch segmented mother boards which span the top and bottom 100 inch width of the chamber. Special power busses with high distributed capacitance are utilized to supply power to the amplifier-discriminator circuits.

Linear Circuits

The amplifier at each end of the delay-line has a 90 to 100Ω input impedance which closely matches the characteristic impedance of the delay-line/ transmission interface. Figure 1 illustrates the cellular structure of the system and highlights the transmission interface.

The signals are routed with shielded twisted pair cable (Belden's Datalene

[1] M. Atac and J. Urish, Nucl. Instr. and Meth. 156 (1978) 163-168

#9730). The cable has a 100Ω nominal impedance and a velocity of propagation similar or better than coaxial cable. The balanced delay line necessitates twin-ax and either a differential input amplifier or a balun matching transformer. The balun is used with a single ended input amplifier to maintain an optimum signal to noise ratio.

The transfomer required magnetic shielding due to the proximity of the Chicago Cyclotron Magnet. A small steel can offers approximately 2kG of effective shielding.

Figure 2 shows the balun and amplifier. The line terminator is composed of a 91Ω carbon resistor and a common-base transistor stage. This circuit was used because of its low input impedance and excellent r.f. properties. The input impedance of the common-base stage was further reduced with the addition of negative feedback. In an attempt to minimize noise and noise amplification the input stage employs rather low value resistances. Transistor Q_2 provides voltage gain and impedance matching to Q_3 which supplies current gain for feedback and drive to the voltage buffer Q_4. Transistor Q_2 and Q_3 are a.c. coupled to avoid Q_1 generated d.c. drift and enhance high frequency response. The feedback network which consists of R_6, and R7-C4 improves noise rejection and high frequency performance.

The amplifier exhibits a very linear response which is essential for delay-line signal processing. Delay-line signals can vary by 2:1 depending on the event position. The amplifier has a 30 dB dynamic range ensuring a solid discriminator signal regardless of far-end or near-end events.

The anode signal is amplified with 2/3 of a MC 10216, (Figure 3). The first stage is biased for linear operation with a resistive divider. The strength of the anode signal can easily saturate a three stage MC 10216 amplifier. Saturation or near-saturation operation must be avoided to maintain wide range discrimination and fast response. Dual anode amplifier-discriminator circuits are required for left-right event detection per chamber channel.

ECL Circuits

The delay-line amplifier-discriminators are polarity sensitive. The MC 10216 is operated as a very fast positive or negative pulse comparator. The external programming voltage is converted to the ECL threshold level with a high impedance transistor buffer. Both the positive and negative comparators are referenced by the buffer. The buffer has a +6 to +8V input range with 6V determining the minimum sensitivity and 8V the maximum. The reference voltages are derived via a balance potentiometer. Another potentiometer is used to zero-out the board-to board threshold variations. (See Figure 2).

The comparators track well over a 20 dB range, but at the large signal end of the range they begin to diverge significantly because of amplifier unsymmetry near saturation.

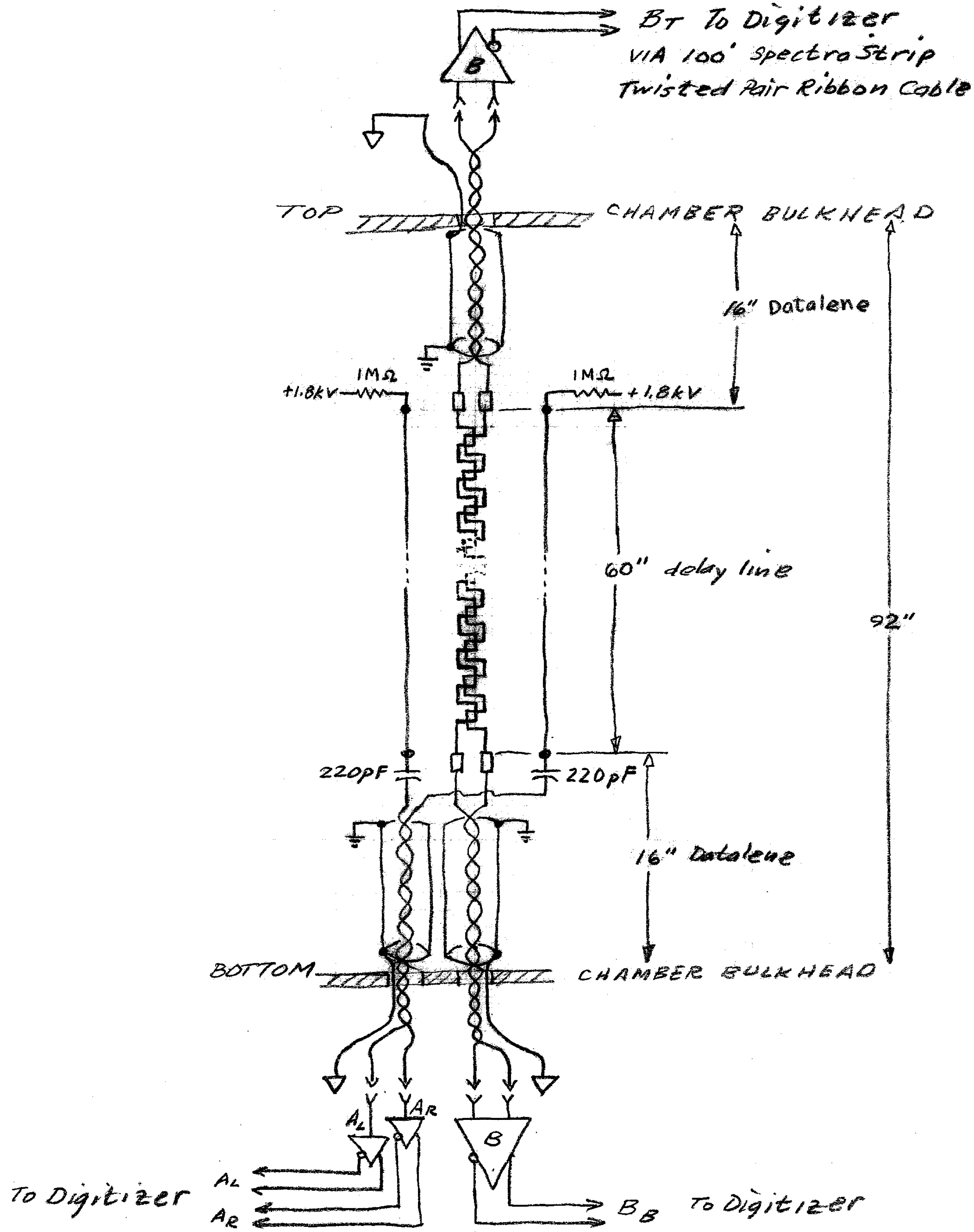
The discriminator outputs are resistively summed at the input of another ECL receiver configured as a voltage controlled monostable multivibrator. The multivibrator produces a 50 ns to 200 ns pulse, dependent upon the remote programming voltage. A Schottky diode provides a fast discharge path for the timing capacitor enabling it to recover quickly during repeated pulsing. The programming voltage is buffered with a transistor stage similar to the threshold buffer. Resistor selection determines the card-to-card pulse width matching to $\pm$ 10%.

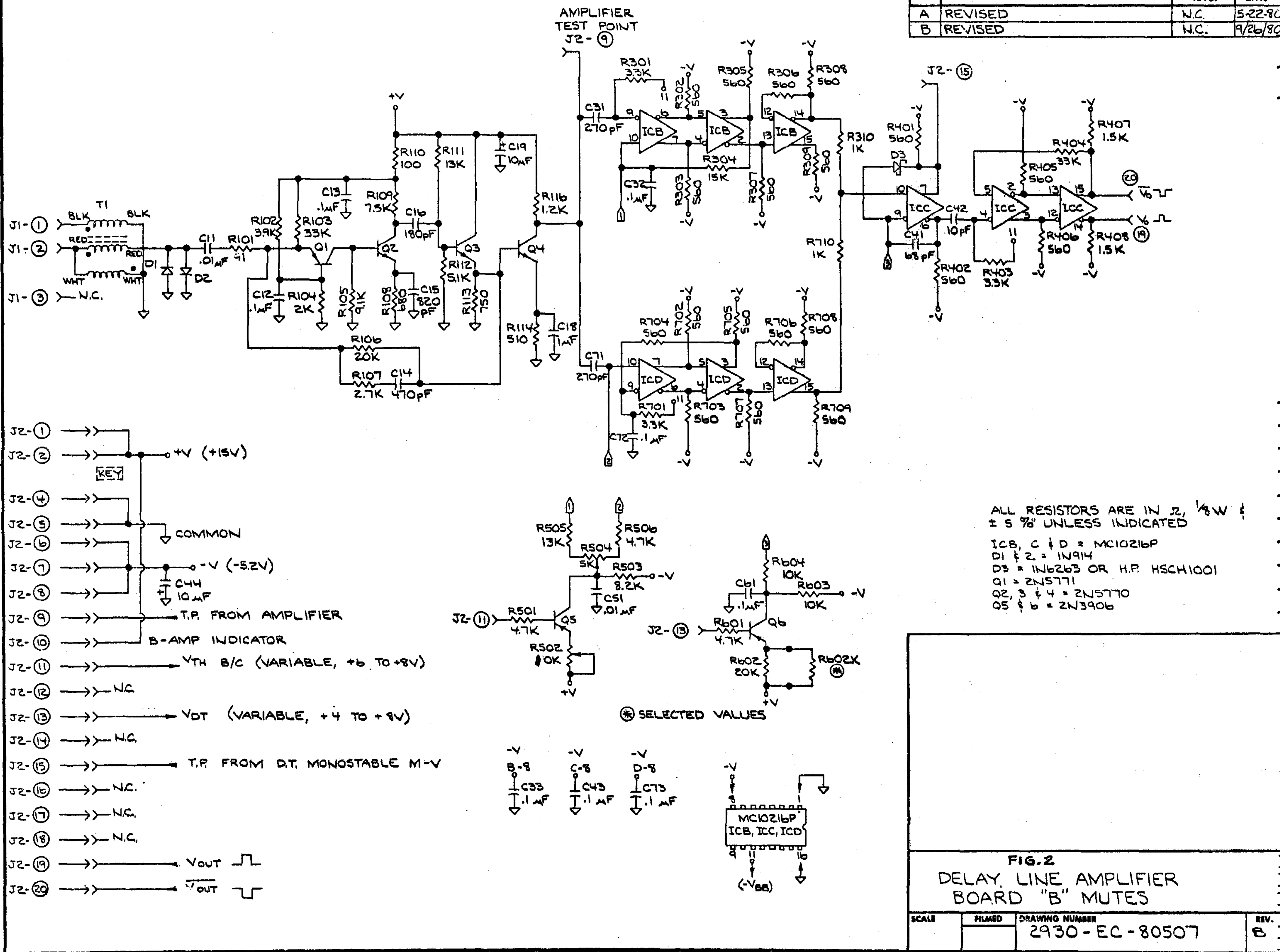
The output cable driver generates a 20 to 35 ns wide pulse with minimum width being determined by cable attenuation. Pulses less than 20 ns require capacitor padding or substitution.

The anode amplifiers unipolar and only require positive comparators. The remaining cirucits (Firgure 3) are identical to those described above.

FERMILAB ENGINEERING NOTE	SECTION	PROJECT	SERIAL-CATEGORY	PAGE
	V	E-610	TM-999 2562.000	4

SUBJECT	NAME	DATE	REVISION DATE
Drift Chamber Cellular Circuit FIG. 1	ARD	9-80	





REV.	DESCRIPTION	DRAWN / APPD.	DATE
A	REVISED	N.C.	5-22-80
B	REVISED	N.C.	9/26/80

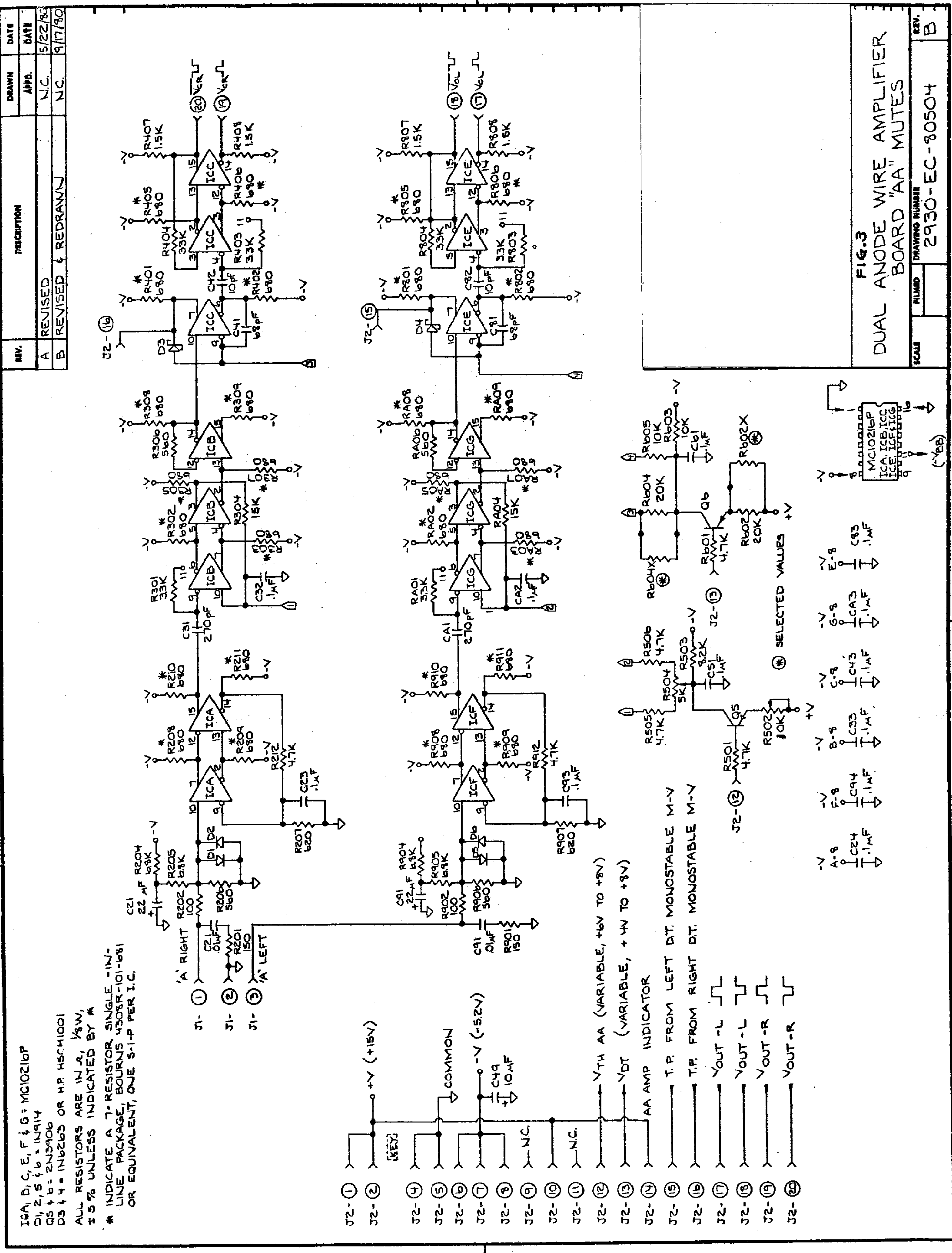
ALL RESISTORS ARE IN Ω, 1/8 W & ± 5 % UNLESS INDICATED

ICB, C & D = MC10216P
D1 & 2 = 1N914
D3 = 1N6263 OR H.P. HSCH1001
Q1 = 2N5771
Q2, 3 & 4 = 2N5770
Q5 & 6 = 2N3906

FIG. 2

DELAY LINE AMPLIFIER BOARD "B" MUTES

SCALE	FILMED	DRAWING NUMBER	REV.
		2930-EC-80507	B


REV. | DESCRIPTION | DRAWN APPD. | DATE
A | REVISED | N.C. | 5/22/80
B | REVISED & REDRAWN | N.C. | 9/17/80
FIG. 3
DUAL ANODE WIRE AMPLIFIER BOARD "AA" MUTES
DRAWING NUMBER 2930-EC-80504
REV. B
AM
ICA, B, C, E, F & G = MC10216P
D1, 2, 5 & 6 = 1N914
Q5 & 6 = 2N3906
D3 & 4 = 1N6263 OR H.P. HSCH1001
ALL RESISTORS ARE IN Ω, 1/8W, ±5% UNLESS INDICATED BY *
* INDICATE A 7-RESISTOR SINGLE-IN-LINE PACKAGE, BOURNS 4308R-101-681 OR EQUIVALENT, ONE S-I-P PER I.C.
(*) SELECTED VALUES
J1-1 'A' RIGHT
J1-3 'A' LEFT
J2-1, J2-2 +V (+15V)
KEY
J2-4, J2-5, J2-6 COMMON
J2-7 -V (-5.2V)
J2-8, J2-9 N.C.
J2-10, J2-11 N.C.
J2-12 V_{TH} AA (VARIABLE, +6V TO +8V)
J2-13 V_{DT} (VARIABLE, +4V TO +8V)
J2-14 AA AMP INDICATOR
J2-15 T.P. FROM LEFT D.T. MONOSTABLE M-V
J2-16 T.P. FROM RIGHT D.T. MONOSTABLE M-V
J2-17 V_{OUT} -L
J2-18 V_{OUT} -L
J2-19 V_{OUT} -R
J2-20 V_{OUT} -R
MC10216P ICA, ICB, ICC, ICE, ICF, ICG
($-V_{BB}$)